Yield Enhancement Approach Using Monte Carlo Simulation in SPICE

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Abstract - **In the present paper, an approach is proposed to automated yield enhancement of analog circuits. It is based on the prediction of the limits of the performance shift using Monte Carlo simulation. The yield and the shifted design parameters, which enhance the yield, are calculated using postprocessing in the graphical analyzer *Probe*. The macrodefinitions realizing the proposed procedure for the yield enhancement, are presented. To evaluate the approach a band-pass filter is used as a design example.**

Keywords – **Yield enhancement, Analog circuits, PSpice simulatior, Monte Carlo analysis.**

I. Introduction

The initial design of analog circuits is carried out using nominal circuit parameters. When the electronic circuit is manufactured, the performance deviates from that for the nominal design. This leads to performance shift and the circuit may fail to meet the performance specifications. In order to assess the performance degradation, the yield is investigated.

A number of methods are developed to calculate the circuit yield [1-4]. Monte Carlo and worst-case approaches are proposed in [2] to yield enhancement. They are implemented in the developed in [2] design tool.

In the present paper, an approach is developed to automated yield enhancement of analog circuits based on Monte Carlo simulation using general-purpose analysis programs. The approach is based on the prediction of the limits of the performance shift of the circuit. The procedure for the yield enhancement is realized using postprocessing in the graphical analyzer *Probe*. The corresponding macrodefinitions are presented for selection of the circuit variants that meet the design specifications and for the yield calculation. The shifted design parameters that enhance the yield, are calculated from the histograms built in *Probe*. To evaluate the approach a band-pass filter is used as a design example.

II. Performance Determination

The investigated performance metrices are denoted by P_i, $i = 1, 2,\ldots, m$. The metrics P_i can be magnitude, phase margin, bandwidth, center frequency, etc. The design parameters are x_i, $i = 1, 2,\ldots, n$.

The following inequalities are defined in order to meet the design specifications:

$$P_{low,i} \le P_i \le P_{hi,i} \tag{1}$$

$$x_i = x_{nom,i} + \varepsilon_{tol,i} + \varepsilon_{sh,i} \ , \tag{2}$$

where $P_{low,i}$ and $P_{hi,i}$ are the lower and the higher limits of the performance specifications, $x_{nom,i}$ is the nominal design parameter, $\varepsilon_{tol,i}$ is the design tolerance and $\varepsilon_{sh,i}$ is the shift of $x_{nom,i}$. The parameters $\varepsilon_{tol,i}$ and $\varepsilon_{sh,i}$ are defined as statistical parameters with uniform distribution.

Performing *Monte Carlo* simulation, the design parameter x_i is changed statistically from its nominal value $x_{nom,i}$ with the design tolerance $\varepsilon_{tol,i}$ and the shift $\varepsilon_{sh,i}$ according to (2).

III. Yield Determination

The inequalities (1) are tested and the circuit variants, satisfying the specifications, are selected. The number of the correct variants n_{cor} meeting all specifications P_i, i=1,2,…,m, is obtained. The yield Y is defined in the form:

$$Y = \frac{n_{cor}}{n_{tot}} \% \ , \tag{3}$$

where n_{tot} is the total number of *Monte Carlo* runs.

In order to obtain the number of the variants that fail to meet the performance specifications, the following parameters are calculated:

$$ena_{low,i} = \begin{cases} 1 \text{ for } P_i \ge P_{low,i} \\ 0 \text{ for } P_i < P_{low,i} \end{cases} , \tag{4}$$

$$ena_{hi,i} = \begin{cases} 1 \text{ for } P_i \le P_{hi,i} \\ 0 \text{ for } P_i > P_{hi,i} \end{cases} . \tag{5}$$

The parameters $ena_{low,i}$ and $ena_{hi,i}$ are calculated using the expressions:

$$ena_{low,i} = \frac{1}{2}\left(\text{sign}\left(P_i - P_{low,i}\right) + 1\right), \tag{6}$$

$$ena_{hi,i} = \frac{1}{2}\left(\text{sign}\left(P_{hi,i} - P_i\right) + 1\right), \tag{7}$$

where *sign*( ) is the sign of the argument.

The parameter *ena* is calculated in the form:

$$ena_i = ena_{low,i} \, . \, ena_{hi,i} \ . \tag{8}$$

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The parameter $ena_i = 1$ if the inequality (1) is satisfied, otherwise $ena_i = 0$. Finally, the parameter *ena* is obtained in the form:

$$ena = \prod_{i=1}^{m} ena_i \ . \qquad (9)$$

The parameter $ena = 1$ if all specifications are satisfied, otherwise $ena = 0$.

The yield *Y* is calculated from (3) giving the percentage of variants, meeting all specifications P_i, $i = 1,2,\ldots,m$. It is obtained from the histogram of *ena* as shown in Fig. 1. This histogram gives automatically the percentage of the variants that meet the requirements (1) (the yield *Y*) for *ena* = 1. For the example shown in Fig. 1, *Y* = 89.1% . The percentage of the failed variants (100-*Y*) is obtained for $ena = 0$.

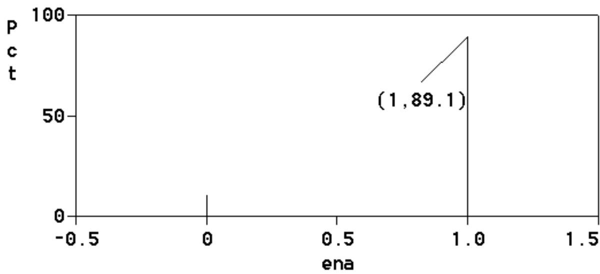

Fig. 1. Determination of the yield *Y* from the histogram of *ena*

IV. Automated Procedure for the Yield Determination using PSpice

The extended possibilities of the *PSpice*-like general-purpose circuit simulators allow to generate statistically the worst-case limits of design parameters meeting the set of performance specifications, taking into account the tolerance or process deviation $\varepsilon_{tol,i}$, together with the shift $\varepsilon_{sh,i}$ of the nominal value $x_{nom,i}$. This is accomplished using *Monte Carlo* simulation, defining uniform distribution for the statistical characteristics $\varepsilon_{tol,i}$ and $\varepsilon_{sh,i}$.

The corresponding histograms for the yield *Y* (Fig. 1) and for the shifted design parameters x_i are obtained. As a result, the new worst case limits $x_{i,\min}$ and $x_{i,\max}$ are calculated from these histograms. The procedure is performed iteratively. The new nominal values x_i, enhancing the yield *Y* at the current iteration step of the algorithm, are calculated as a mean value:

$$x_i = 0.5\left(x_{i,\min} + x_{i,\max}\right) \qquad (10)$$

The yield *Y* and the shifted design parameters are obtained from (9) and (10) using postprocessing of the simulation results in the graphical analyzer *Probe*.

The procedure is demonstrated for the yield enhancement of the band-pass filter shown in Fig. 2. The nominal values are obtained according to the design procedure assuming ideal operational amplifiers (Fig. 2a). The circuit with real operational amplifiers is shown in Fig. 2b. The defined design tolerances are 1% for the resistors and 2% for capacitors. The performance metrices $P_i, i = 1,2,3$ are the center frequency F_o, the bandwidth *B*, and the maximal magnitude of the gain *G*. The frequency responses of the filter gain are shown in Fig. 3 for the case of ideal OpAmps (solid line – curve 1) and for the case of real OpAmps (dashed line - curve 2). The tolerance fields of the gain *G* are presented in Fig. 4a for the case with ideal OpAmps and in Fig. 4b for the case with real OpAmps.

The following specifications are defined for F_o, *B* and *G* using macrodefinitions in *Probe*:

– bandwidth *B*:

```
Bmin = 2210
Bmax = 3330
```

– center frequency F_o :

```
Fomin = 11100
Fomax = 11570
```

– gain *G*:

```
Gmin = 0.8
Gmax = 1.23
```

These specifications ensure 100% yield for the case 1 (Fig. 4a). The same metrices fail to meet the defined specifications for the case 2 (Fig. 4b) and the yield is 0%.

Applying simultaneously statistical deviations $\varepsilon_{tol,i}$ and $\varepsilon_{sh,i}$ with uniform distribution to the design parameters x_i according to (2), the total yield Y_t is obtained. The following macrodefinitions are used:

1. Calculation of *B* and F_o

```
B = Bandwidth(Vdb(OUT),3)
Fo = CenterFreq(Vdb(OUT),3)
```

2. Calculation of $ena_{low,i}$, $ena_{hi,i}$ from (6) and (7):

```
ena_B_l = 0.5*(sgn(B-Bmin)+1)
ena_B_h = 0.5*(sgn(Bmax-B)+1)
ena_Fo_l = 0.5*(sgn(Fo-Fomin)+1)
ena_Fo_h = 0.5*(sgn(Fomax-Fo)+1)
ena_G_l = 0.5*(sgn(max(V(OUT))-Gmin)+1)
ena_G_h = 0.5*(sgn(Gmax-max(V(OUT)))+1)
```

3. Calculation of ena_i from (8):

```
ena_B = ena_B_l*ena_B_h
ena_Fo = ena_Fo_l*ena_Fo_h
ena_G = ena_G_l*ena_G_h
```

2. Calculation of *ena* from (9):

```
ena = ena_B*ena_Fo*ena_G
```

The *Probe* function **sgn( )** is used to obtain the sign of the argument.

The histogram of *ena* is built to calculate the yield. The percentage of the variants, meeting the specifications corresponds to *ena* = 1. The total yield Y_t is calculated for the design parameters x_i from (2) defined with design tolerance $\varepsilon_{tol,i}$ and shift $\varepsilon_{sh,i}$. The yield *Y* is obtained taking into account the design tolerance $\varepsilon_{tol,i}$ without shift.

The yield values, calculated for the nominal design parameters, are $Y^{(1)} = 0\%$ and $Y_t^{(1)} = 1.6\%$. Three *Monte Carlo* iterations are performed and the measures $Y_t^{(i)}$ and $Y^{(i)}$ at each iteration step are calculated. They are presented in Table I. The final value of the yield *Y* = 89.1% is calculated with the obtained at the step 3 design parameters x_i.

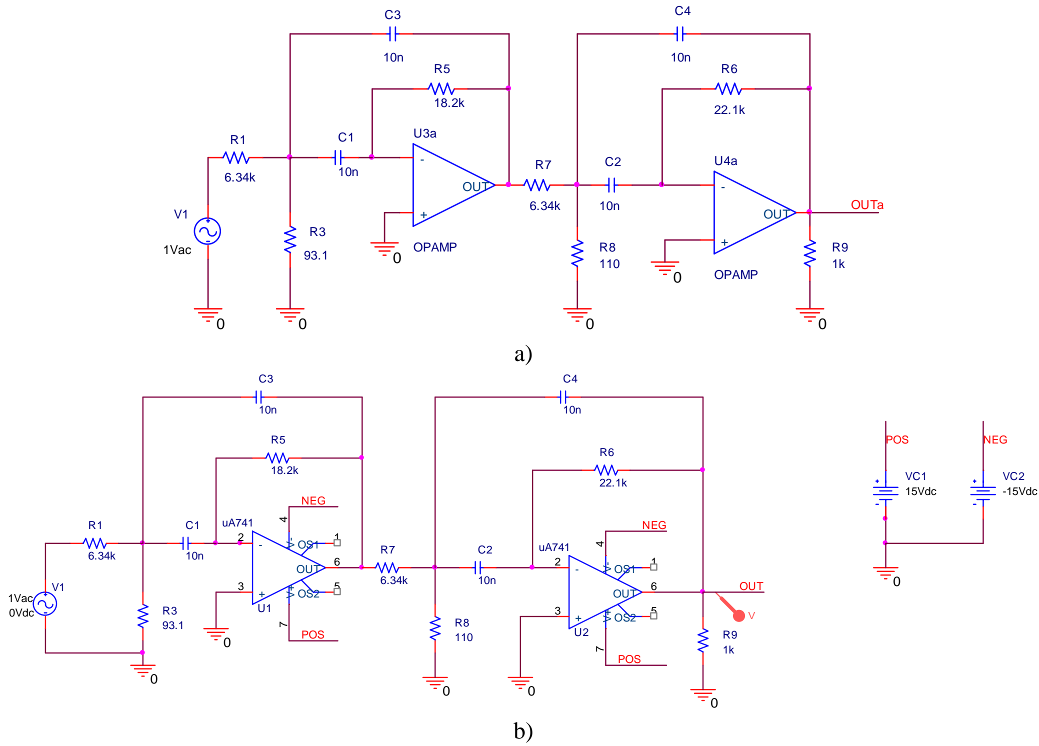

Fig. 2. The example band-pass filter

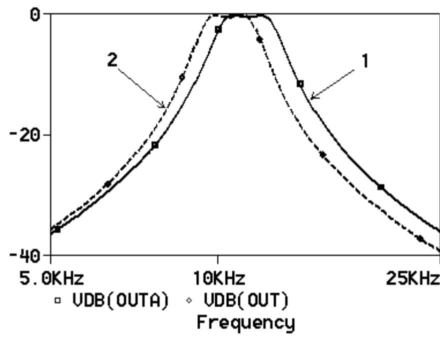

Fig. 3. Frequency response of the gain G

The recalculated parameter values *R*, *L* and *C* are obtained in *Probe* using the component equations:

$$R = \left|\frac{\dot{V}_R}{\dot{I}_R}\right| ; \; L = \left|\frac{\dot{V}_R}{\omega \dot{I}_R}\right| ; \; C = \left|\frac{\dot{I}_C}{\omega \dot{V}_C}\right| \tag{11}$$

They are calculated using the following predefined macrodefinitions in *Probe*:

```
VALR(RR) = max(m(V(RR:1,RR:2)/I(RR)))
VALL(LL) = max(m(V(LL:1,LL:2)/(I(LL)
     *2*pi*frequency)))
VALC(CC) = max(m(I(CC)/(V(CC:1,CC:2)
     *2*pi*frequency)))
```

The. frequency response of the gain G after the yield enhancement is shown in Fig. 5, where the curve 1 corresponds to the gain with ideal OpAmps, curve 2 – to the gain with real OpAmps and initial values for the nominal parameters and curve 3 is the final characteristic for G after applying the yield enhancement procedure.

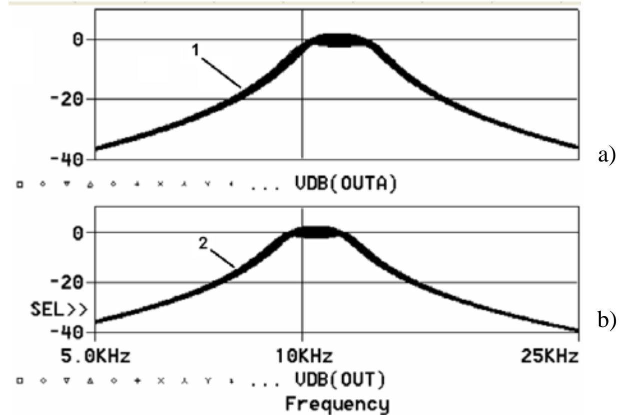

Fig. 4. Tolerance fields of the gain G (a) for the case with ideal OpAmps and (b) for the case with real OpAmps.

TABLE I. PERCENTAGE OF THE VARIANTS MEETING THE SPECIFICATIONS (YIELD)

Iteration step	1	2	3
$Y_t^{(i)}$	1.6%	11.2%	14.8%
$Y^{(i)}$	0	11.7%	68.4%

The yield increases from 0% (for case 2) to 89.1% (for case 3). The initial nominal values and the final values, obtained at iteration 3, are shown in Table II.

The histograms of the parameter C_1 obtained in *Probe* for the calculation of $Y_t^{(k)}$ at iterations k = 1, 2, 3, are presented in Fig. 6. The final result for the tolerance range of C_1 is also shown in Fig. 6.

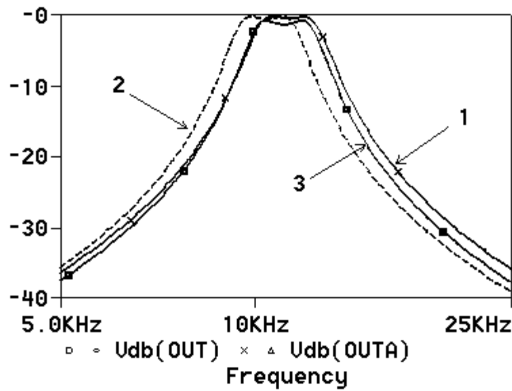

Fig. 5. Frequency response of the gain G after the yield enhancement

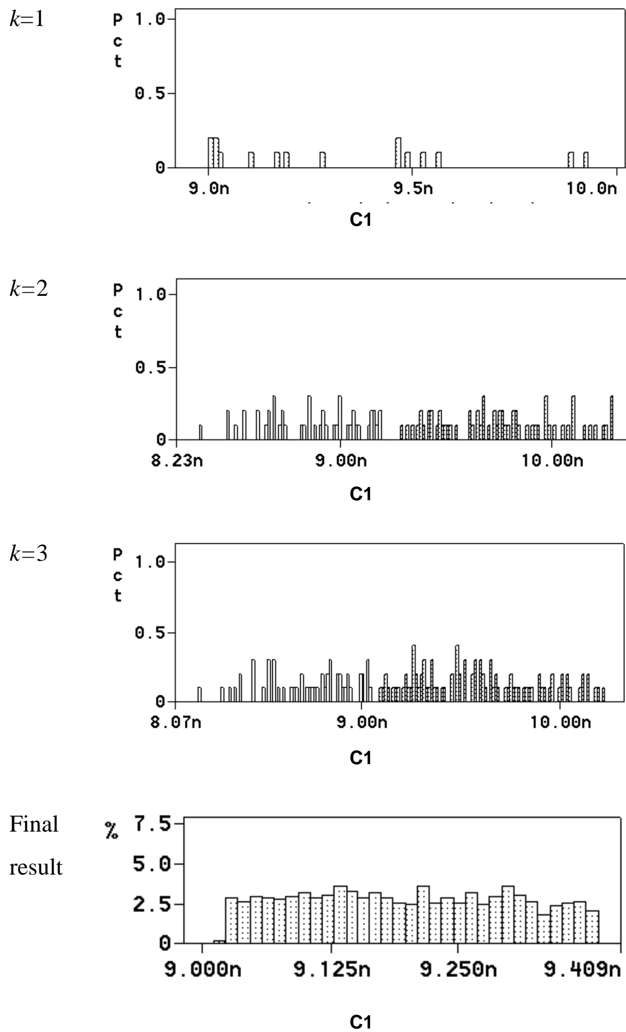

Fig. 6. Histograms of the parameter C_1

TABLE II. INITIAL AND FINAL CIRCUIT PARAMETERS

Parameter	Initial	Final
R_1	6.34 kΩ	6.412 kΩ
R_3	93.1 Ω	92.58 Ω
R_5	18.2 kΩ	18.1 kΩ
R_6	22.1 kΩ	22.19 kΩ
R_7	6.34 kΩ	6.283 kΩ
R_8	110 Ω	109.5 Ω
R_9	1k Ω	1.009 kΩ
C_1	10nF	9.2 nF
C_2	10nF	9.498 nF
C_3	10nF	9.498 nF
C_4	10nF	9.31 nF

V. CONCLUSION

An approach has been developed to automated yield enhancement of analog circuits. It is performed using statistical analysis implemented in the general-purpose PSpice-like circuit simulators. The method is based on prediction of the worst-case limits for the set of performance metrices. The yield and the shifted design parameters, which enhance the yield, are calculated using postprocessing in the graphical analyzer *Probe*. The corresponding *Probe* macrodefinitions for the realization of the yield enhancement procedure are presented.

VI. ACKNOWLEDGEMENT

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